CCD Adapter Module

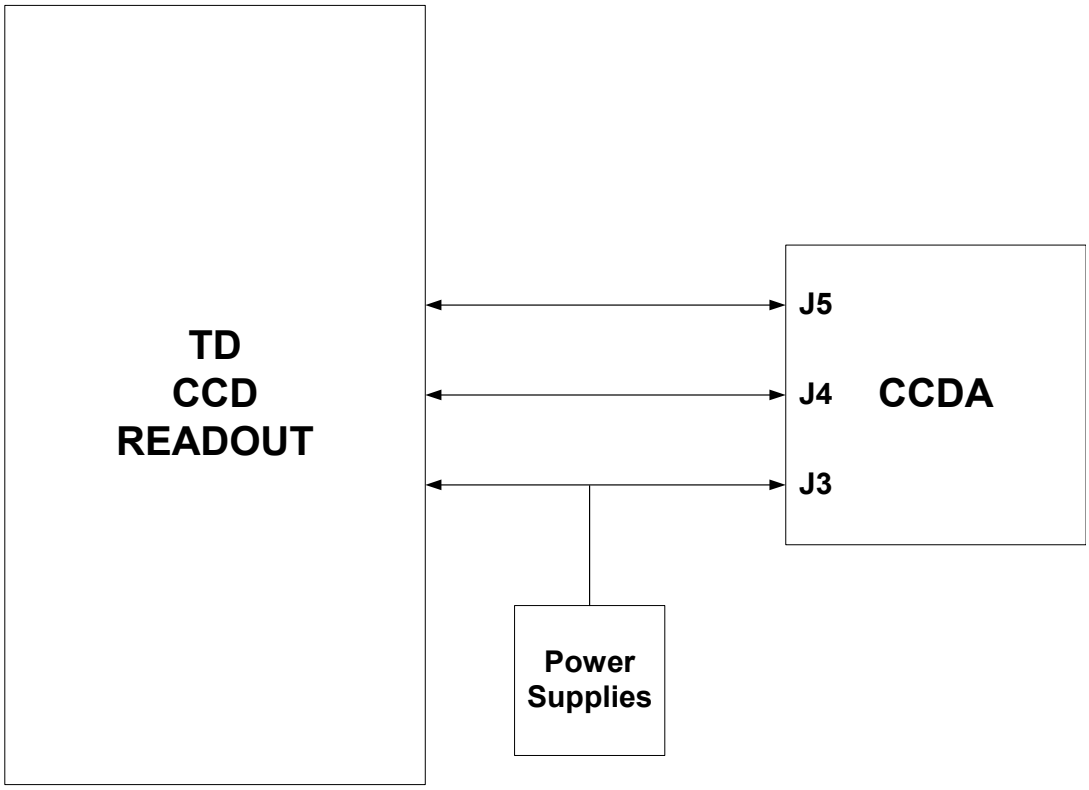
Introduction

The CCD Adapter (CCDA) has been designed to accept the picture frame package of the LBL small CCD. The CCDA derives the majority of its control and voltage levels from the CCD readout system designed by and built by Tom Droege (TD). The purpose of this note is to document how we must program that system in order to readout the LBL CCD.

Control Signals and DAC Voltages

The CCDA relies on three 25-pin cables to bring control signals from the TD CCD Readout modules. The first two cables, J5 and J4, are cables which come from the TD ADC modules. Two cables are used to provide for readout from each of two amplifiers on the LBL CCD.

The third cable, J3, consists of various DAC voltages and control signals which must be gathered from various sections of the TD system as well as some special power rails to provide the substrate voltage (+80V) and Vdd (-22V).



Connector J5 – 26 conductor cable between CCDA and Tom's ADC Board

Pin	Signal	Pin	Signal
1	GND	14	RX
2	HX1	15	HX3
3	VHL	16	HX2
4	VHH	17	-5V
5	VRL	18	RY
6	-15V	19	VRH
7	+5V	20	VX3
8	+15V	21	VX1
9	VSS	22	VX2
10	VVH	23	VDD
11	VVL	24	HQ
12	TCCD	25	VOUT
13	TW		

Signal Definition

TD Signal	TD Signal Source	Signal Definition
GND	ADC board	
HX1[1]	ADC board (H PROM)	Horizontal Clock 1
VHL	ADC board	DAC voltage – horizontal clock low voltage level (-4V)
VHH	ADC board	DAC voltage – horizontal clock high voltage level (+6V)
VRL	ADC board	DAC voltage – reset gate low voltage level (-6V)
-15V	ADC board	
+5V	ADC board	
+15V	ADC board	
VSS	ADC board	
VVH	ADC board	DAC voltage – vertical clocks and transfer gate high voltage level (+5V)
VVL	ADC board	DAC voltage – vertical clocks and transfer gate low voltage level (-3V)
TCCD	ADC board	Temperature Transducer (AD590) analog readout
TW	ADC board	Temperature Transducer (AD590) analog readout
RX[1]	ADC board (H PROM)	Reset Gate
HX3[1]	ADC board (H PROM)	Horizontal Clock 3
HX2[1]	ADC board (H PROM)	Horizontal Clock 2
-5V	ADC board	
RY[1]	ADC board (H PROM)	Contols switch which resets (grounds) video op amp input when set to high level
VRH	ADC board	DAC voltage – reset gate high voltage level (0V)
VX3[1]	ADC board (V PROM)	Vertical Clock 3
VX1[1]	ADC board (V PROM)	Vertical Clock 1
VX2[1]	ADC board (V PROM)	Vertical Clock 2
VDD	ADC board	not used
HQ	ADC board	Channel 1 video signal return
VOUT	ADC board	Channel 1 video signal out

Note 1: All clock and control signals operate such that:
control signal = 0 gates through low voltage level
control signal = 1 gates through high voltage level

Connector J4 – 26 conductor cable between CCDA and Tom's ADC Board

Pin	Signal	Pin	Signal
1	GND	14	
2		15	
3		16	
4		17	-5V
5		18	
6	-15V	19	
7	+5V	20	
8	+15V	21	
9	VSS	22	
10		23	
11		24	HQ
12		25	VOUT
13			

Signal Definition

TD Signal	TD Signal Source	Signal Definition
GND	ADC board	
-15V	ADC board	
+5V	ADC board	
+15V	ADC board	
VSS	ADC board	
-5V	ADC board	
HQ	ADC board	Channel 2 video signal return
VOUT	ADC board	Channel 2 video signal out

Connector J3 – 26 conductor cable between CCDA and Tom's ADC Board

Pin	Signal	Pin	Signal
1	+80V	14	
2	VSS	15	
3	-30V	16	
4	VSS	17	
5	-22V	18	
6	VSS	19	
7		20	SPARE_H
8		21	SPARE_V
9		22	TEMP_COMMAND_0
10	STAMP_P0	23	TEMP_COMMAND_1
11	STAMP_P1	24	TEMP_COMMAND_2
12	STAMP_P2	25	TEMP_COMMAND_3
13			

Signal Definition

TD Signal	TD Signal Source	Signal Definition
+80V		used for substrate bias
VSS		
-30V		used to help produce Vdd (-22V)
VSS		
-22V		used to help produce Vdd (-22V)
VSS		
STAMP_P0	Stamp Board (34 pin connector to Motor Board)	control signal used to enable all clock and gate voltages =0 switch is open =1 switch passes through clock and gate voltages
STAMP_P1	Stamp Board (34 pin connector to Motor Board)	control signal used to ground n+ guard n+ guard normally floats, grounded for erase =0 switch is open =1 n+ guard is grounded
STAMP_P2	Stamp Board (34 pin connector to Motor Board)	control signal used to turn on Vdd =0 switch is open =1 Vdd is gated through to CCD
SPARE_H	Scan Board – H output header (PROM output)	used to control Summing Well (SW) gate
SPARE_V	Scan Board – V output header (PROM output)	used to control Transfer Gate (TG)
TEMP_COMMAND_0	Stamp Board – DAC output pin	DAC voltage – SW gate high voltage level (+5V)
TEMP_COMMAND_1	Stamp Board – DAC output pin	DAC voltage – SW gate low voltage level (-5V)
TEMP_COMMAND_2	Stamp Board – DAC output pin	DAC voltage – Vr (-12.5V)
TEMP_COMMAND_3	Stamp Board – DAC output pin	DAC voltage – Vopg (+2.16V)

Steps for using CCDA

Turn on Power
- +80V (Substrate voltage)
- +/-5V, +/-15V
- -30V, -22V (Vdd)

Initial levels of Control signals
- STAMP_P0 = 0 to hold off clock and gate voltages
- STAMP_P1 = 0 to leave n+guard floating
- STAMP_P2 = 0 to leave Vdd turned off

Start-up
- Turn on Vdd bu setting STAMP_P2 =1
- Set all DAC voltages
  - VHL = -4V
  - VHH = +6V
  - VRL = -6V
  - VRH = 0V
  - VVH = +5V
  - VVL = -3V
  - TEMP_COMMAND_0 = +5V
  - TEMP_COMMAND_1 = -5V
  - TEMP_COMMAND_2 = -12.5V
  - TEMP_COMMAND_3 = +2.16V
- Turn on clock and gate voltages by setting STAMP_P0 =1

Run acquisition – assumes PROMS properly programmed

Vertical PROM Definition

Bit	TD Signal Name	Special CCDA Application
0	START H SCAN	
1	SPARE V	Transfer Gate (TG)
2	BLOCK DONE	
3	VX3	Vertical Clock 3
4	VX1	Vertical Clock 1
5	VX2	Vertical Clock 2
6	STOPV SCAN	
7	PAUSE V SCAN	

Horizontal PROM Definition

Bit	TD Signal Name	Special CCDA Application
0	HX2	Horizontal Clock 2
1	HX1	Horizontal Clock 1
2	CONVERT	
3	DATA	
4	IRESET	
5	SELECT ADC 0	
6	SELECT ADC 1	
7	SPARE H	Summing Well (SW)
8	CABLE CLOCK	
9	INTEGRATE	
10	BYTE	
11	RX	Reset Gate (RG)
12	HX3	Horizontal Clock 3
13	RY	Resets (grounds) video op amp input
14	CONTINUE V SCAN	
15	STOP H SCAN	

Dual Amplifier Readout

A couple of jumpers on the CCDA control whether the U, L or both output amplifiers of the LBL CCD are read out.

J7	**J8**	**Function**
ON	ON	dual readout
ON	OFF	U amp readout
OFF	ON	L amp readout